



PTO/SB/08a (03-03)

Approved for use through 07/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/786,643
				Filing Date	2/25/2004
				First Named Inventor	Cheng, et al.
				Art Unit	2826
				Examiner Name	Quinto, Kevin
				Attorney Docket Number	TSM03-0698
Sheet	1	of	6		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
K2	1	US-4,069,094	01-17-1978	Shaw et al.	
	2	US-4,314,269	02-02-1982	Fujiki	
	3	US-4,497,683	02-05-1985	Celler et al.	
	4	US-4,631,803	12-30-1986	Hunter et al.	
	5	US-4,846,799	08-07-1990	Blake et al.	
	6	US-5,155,571	10-13-1992	Wang et al.	
	7	US-5,378,919	01-03-1995	Ochial	
	8	US-5,447,884	09-05-1995	Fahey et al.	
	9	US-5,461,250	10-24-1995	Burghartz et al.	
	10	US-5,479,033	12-26-1995	Baca et al.	
	11	US-5,534,713	07-09-1996	Ismail et al.	
	12	US-5,629,544	05-13-1997	Voldman et al.	
	13	US-5,714,777	02-03-1998	Ismail et al.	
	14	US-5,763,315	06-09-1998	Benedict et al.	
	15	US-5,789,807	08-04-1998	Correale Jr.	
	16	US-5,811,857	09-22-1998	Assaderaghi et al.	
	17	US-6,008,095	12-28-1999	Gardner et al.	
	18	US-6,015,993	01-18-2000	Voldman et al.	
	19	US-6,046,487	04-04-2000	Benedict et al.	
	20	US-6,059,895	05-09-2000	Chu et al.	
	21	US-6,111,267	08-29-2000	Fischer et al.	
	22	US-6,222,234 B1	04-24-2001	Imai	
	23	US-6,232,183 B1	05-15-2001	Voldman et al.	
	24	US-6,256,239 B1	07-03-2001	Akita et al.	
	25	US-6,258,664 B1	07-10-2001	Reinberg	
	26	US-6,291,321 B1	09-18-2001	Fitzgerald	
	27	US-6,294,834 B1	09-25-2001	Yeh et al.	
	28	US-6,339,232 B1	01-15-2002	Takagi	
	29	US-2002/0031890 A1	03-14-2002	Watanabe et al.	
	30	US-6,358,791 B1	03-19-2002	Hsu et al.	
	31	US-6,387,739 B1	05-14-2002	Smith III	
	32	US-6,396,137 B1	05-28-2002	Klughart	
	33	US-6,407,408 B1	06-18-2002	Tezuka	
	34	US-2002/0076899 A1	06-20-2002	Skotnicki et al.	
	35	US-2002/0074598 A1	06-20-2002	Doyle et al.	
	36	US-6,413,802 B1	07-02-2002	Hu et al.	
	37	US-6,414,355 B1	07-02-2002	An et al.	
	38	US-6,429,061 B1	08-06-2002	Rim	
	39	US-6,448,114 B1	09-10-2002	An, et al.	

Examiner Signature	Kevin Quinto	Date Considered	4/28/05
-----------------------	--------------	--------------------	---------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP §01.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Under the Paperwork Reduction Act of 1985, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	10/786,643
				Filing Date	2/25/2004
				First Named Inventor	Cheng, et al.
				Art Unit	2826
				Examiner Name	Quinto, Kevin
				Attorney Docket Number	TSM03-0698
Sheet	2	of	6		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
72	40	US-2002/0125471 A1	09-12-2002	Fitzgerald et al.	
	41	US-2002/0140031 A1	10-03-2002	Rim	
	42	US-2002/0153549 A1	10-24-2002	Laibowitz et al.	
	43	US-6,475,838 B1	11-05-2002	Bryant et al.	
	44	US-6,475,869 B1	11-05-2002	Yu	
	45	US-6,489,684 B2	12-03-2002	Re et al.	
	46	US-2002/0190284 A1	12-19-2002	Murthy et al.	
	47	US-2003/0001219 A1	01-02-2003	Chau et al.	
	48	US-6,518,610 B2	02-11-2003	Yang et al.	
	49	US-2003/0030091 A1	02-13-2003	Bulsara et al.	
	50	US-6,524,905 B2	02-25-2003	Yamamichi et al.	
	51	US-6,525,403 B2	02-25-2003	Inaba et al.	
	52	US-6,555,839 B2	04-29-2003	Fitzgerald	
	53	US-2003/0080361 A1	05-01-2003	Murthy et al.	
	54	US-2003/0080386 A1	05-01-2003	Ker et al.	
	55	US-6,558,998 B2	05-06-2003	Belleville et al.	
	56	US-6,573,172 B1	06-03-2003	En et al.	
	57	US-6,576,528 B2	06-10-2003	Kai et al.	
	58	US-6,600,170 B1	07-29-2003	Xiang	
	59	US-2003/0162348 A1	08-28-2003	Yeo et al.	
	60	US-6,621,131 B2	09-16-2003	Murthy et al.	
	61	US-6,653,700 B2	11-25-2003	Chau et al.	
	62	US-6,657,276 B1	12-02-2003	Karlsson et al.	
	63	US-2003/0227013 A1	12-11-2003	Currie et al.	
	64	US-2004/0018688 A1	01-29-2004	Maszara	
	65	US-2004/0026765 A1	02-12-2004	Currie et al.	
	66	US-2004/0063300 A1	04-01-2004	Chi	
	67	US-6,720,619 B1	04-13-2004	Chen et al.	
	68	US-6,724,019 B2	04-20-2004	Oda et al.	
	69	US-2004/0104405 A1	06-03-2004	Huang et al.	
	70	US-2004/0108598 A1	06-10-2004	Cabral, Jr. et al.	
	71	US-6,759,717 B2	07-08-2004	Sagarwala et al.	
	72	US-6,762,448 B1	07-13-2004	Lin et al.	
	73	US-2004/0173815 A1	09-09-2004	Yeo et al.	
	74	US-6,784,764 B1	09-21-2004	Kamal et al.	
72	75	US-6,803,641 B2	10-12-2004	Papa Rao et al.	

Examiner Signature	Kevin Quinto	Date Considered	11/20/05
--------------------	--------------	-----------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/786,643
				Filing Date	2/25/2004
				First Named Inventor	Cheng, et al.
				Art Unit	2826
				Examiner Name	Quinto, Kevin
				Attorney Docket Number	TSM03-0698
Sheet	3	of	6		

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁰
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
JZ	76	EP 0 683 522 A2	11-22-1995	International Business Machines Corporation		
	77	EP 0 828 296 A2	03-11-1998	International Business Machines Corporation		
	78	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JZ	79	"Future Gate Stack," International Sematech, 2001 Annual Report.	
↓	80	"BEDNAR, T.R., et al. "Issues and Strategies for the Physical Design of System-On-A-Chip ASICs," IBM J. RES. & DEV., Vol. 46, No. 6 (November 2002) pp. 661-674.	
	81	BLAAUW, D., "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.	
JZ	82	CAVASSILAS, N., et al., "Capacitance-Voltage Characteristics of Metal-Oxide-Strained Semiconductor Si/SiGe Heterostructures," Nanotech 2002, Vol. 1, pp. 600-603.	

Examiner Signature	Kevin Quinto	Date Considered	11/20/05
-----------------------	--------------	--------------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			Complete If Known		
			Application Number	10/786,643	
			Filing Date	2/25/2004	
			First Named Inventor	Cheng, et al.	
			Art Unit	2826	
			Examiner Name	Quinto, Kevin	
Sheet	4	of	6	Attorney Docket Number	TSM03-0698

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
<i>72</i>	83	CHANG, L., et al., "Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs," 2002 IEEE Transactions on Electron Devices, Vol. 49, No. 12, December 2002, pp. 2288-2295.		
<i>7</i>	84	CHANG, L., et al., "Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs," IEEE, 2001, 4 pages.		
	85	GÁMIZ, F., et al., "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, July 1, 2002, pp. 288-295.		
	86	GÁMIZ, F., et al., "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, June 3, 2002, pp. 4160-4162.		
	87	GE, C.-H., et al., "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," IEDM (2003) pp. 73-76.		
	88	GHANI, T., et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," IEDM (2003) pp. 978-980.		
	89	HUANG, X., et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pp. 880-886.		
	90	ISMAIL, K, et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, August 2, 1993, pp. 660-662.		
	91	JURCZAK et al., M., "Silicon-on-Nothing (SON) – an Innovative Process for Advanced CMOS," IEEE Transactions on Electron Devices, Vol. 47, No. 11, November 2000, pp. 2179-2187.		
<i>✓</i>	92	JURCZAK, M., et al., "SON (Silicon on Nothing) – A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA," Symposium on VLSI Technology Digest of Technical Papers, 1999, pp. 29-30.		
<i>72</i>	93	LEITZ, C.W., et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Materials Research Society Symposium Proceedings, Vol. 686, 2002, pp. 113-118.		

Examiner Signature	<i>Kevin Quinto</i>	Date Considered	<i>4/20/05</i>
--------------------	---------------------	-----------------	----------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

*Applicant's unique citation designation number (optional). *Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449B/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Application Number	10/785,643
			Filing Date	2/25/2004
			First Named Inventor	Cheng, et al.
			Art Unit	2826
			Examiner Name	Quinto, Kevin
			Attorney Docket Number	TSM03-0698
(Use as many sheets as necessary)				
Sheet	5	of	6	

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
72	94	LEITZ, C.W., et al., "Hole Mobility Enhancements In Strained Si/Si _{1-y} Ge _y P-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown On Relaxed Si _{1-x} Ge _x (x<y) Virtual Substrates," Applied Physics Letters, Vol. 79, No. 25, December 17, 2001, pp. 4246-4248.		
	95	LIU, K.C., et al., "A Novel Sidewall Strained-Si Channel nMOSFET," IEDM, 1999, pp. 63-66.		
	96	MAITI, C.K., et al., "Film Growth and Material Parameters," Application of Silicon-Germanium Heterostructure, Institute of Physics Publishing, pp. 32-42.		
	97	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1, Jan./Feb. 1975, pp. 126-133.		
	98	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers - I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, 1974, pp. 118-125.		
	99	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers - II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks", Journal of Crystal Growth, Vol. 29, 1975, pp. 273-280.		
	100	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers - III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, 1976, pp. 265-273.		
	101	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, January 2002, pp. 7-14.		
	102	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, April 1991, pp. 154-156.		
	103	OOTSUKA, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Application," International Electron Device Meeting, 2000, pp. 575-578.		
72	104	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, 1995, pp. 298-305.		

Examiner Signature	Kevin Quinto	Date Considered	11/20/05
--------------------	--------------	-----------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional). *Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449B/PTO		Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	10/786,643
		Filing Date	2/25/2004
		First Named Inventor	Cheng, et al.
		Art Unit	2826
		Examiner Name	Quinto, Kevin
(Use as many sheets as necessary)		Attorney Docket Number	TSM03-0698
Sheet	6	of	6

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
KJ	105	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
	108	SHIMIZU, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
	107	TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, 2002, pp. 96-97.	
	108	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um ² SRAM Cell," IEDM, December 2002, pp. 61-64.	
	109	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, 1997, pp. 939-941.	
	110	WANG, L.K., et al., "On-Chip Decoupling Capacitor Design to Reduce Switching-Noise-Induced Instability in CMOS/SOI VLSI," Proceedings of the 1995 IEEE International SOI Conference, Oct. 1995, pp. 100-101.	
	111	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM, 1992, pp. 1000-1002.	
	112	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
	113	YANG, F.L., et al., "35nm CMOS FinFETs," Symposium on VLSI Technology Digest of Technical Papers, 2002, pp. 104-105.	
	114	YANG, F.L., et al., "25 nm CMOS Omega FETs," IEDM, 2002, pp. 255-258.	
KJ	115	YEOH, J.C., et al., "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol., Vol. 13, 1998, pp. 1442-1445.	

Examiner Signature	Kevin Quinto	Date Considered	2/28/03
--------------------	--------------	-----------------	---------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional). *Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.